RECONFIGURABLE ANALOG-TO-DIGITAL CONVERTER

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to the field of signal processing and more specifically to a reconfigurable analog-to-digital converter.

BACKGROUND OF THE INVENTION

Analog-to-digital converters (ADCs) are generally configured to operate at specific bandwidth ranges with particular sampling frequency ranges. For example, a pipeline ADC typically operates at a Nyquist frequency, while a sigma-delta modulator may operate at an oversampling frequency range. In some circuit designs, it may be necessary to have an analog-to-digital converter operating at different resolutions. Known techniques for having an ADC operating at different resolutions involve including various ADCs in the design according to the desired resolution. These known techniques, however, may result in a more costly design in some situations.

SUMMARY OF THE INVENTION

In accordance with the present invention, disadvantages and problems associated with previous techniques for processing data packets using markers may be reduced or eliminated.

According to one embodiment, configuring an analog-to-digital converter includes receiving a control signal and an input analog signal at an analog-to-digital converter, where the control signal has either a first state or a second state. The first state is associated with a first configuration and the second state is associated with a second configuration. If the control signal has the first state, the analog-to-digital-converter is configured in the first configuration and a digital signal comprising a first digital signal is generated according to a pipeline conversion. If the control signal has the second state the analog-to-digital converter is configured in the second configuration and the digital signal comprising a second digital signal is generated according to a multi-stage sigma delta modulation conversion. The digital signal is processed to yield a digital output.

Certain embodiments of the invention may provide one or more technical advantages. A technical advantage of one embodiment may be the simplified hardware of a circuit that requires the use of various types of ADC resolution. Another technical advantage of one embodiment may be that by reconfiguring an ADC using a control signal, the reconfiguration may be more efficient.

Certain embodiments of the invention may include none, some, or all of the above technical advantages. One or more other technical advantages may be readily

apparent to one skilled in the art from the figures, descriptions, and claims included herein.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and its features and advantages, reference is now made to the following description, taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a block diagram of one embodiment of a reconfigurable analog-to-digital converter that may be used in accordance with the present invention;

FIGURE 2 is a block diagram of one embodiment of a pipeline configuration that may be used with the reconfigurable analog-to-digital converter of FIGURE 1; and

FIGURE 3 is a block diagram of one embodiment of a multi-stage noise shaping configuration that may be used with the reconfigurable analog-to-digital converter of FIGURE 1.

DETAILED DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention and its advantages are best understood by referring to FIGURES 1 through 3 of the drawings, like numerals being used for like and corresponding parts of the various drawings.

FIGURE 1 is a block diagram of one embodiment of a reconfigurable analog-to-digital converter (ADC) 10 that may be used in accordance with the present invention. In general, reconfigurable ADC 10 may be reconfigured according to a control signal. The control signal may operate to switch the configuration of reconfigurable ADC 10 from a pipeline ADC to a multistage sigma delta (MASH) ADC and vice versa. According to the illustrated embodiment, reconfigurable ADC 10 includes a first stage 12, a middle stage 14, a final stage 16, and a digital logic block 18 coupled as shown in FIGURE 1.

Stages 12, 14, and 16 each includes an integrator, at least one summing node Σ_1 and Σ_2, a multi-bit quantizer (sub-ADC), and a feedback digital to analog converter (DAC). Each stage 12, 14, and 16 is coupled to each other using an interstage gain G so that the coarse output of a previous stage may be fed to a subsequent stage. Reconfigurable ADC 10 may include any number of middle stages 14 without departing from the scope of the invention.

According to the illustrated embodiment, first stage 12 includes a switched integrator 32 that is controlled by a control signal *SDM*. Depending on the status of the control signal, integrator 32 of first stage 12 may operate as a sample/hold circuit or as an integrator. For example, if control signal *SDM* is low, the integrator feedback of first stage 12 is closed thereby configuring

switched integrator 32 into a sample/hold circuit, which may be used in a pipeline ADC configuration as will be more particularly described with reference to FIGURE 2. If control signal *SDM* is high, the integrator feedback of first stage 12 is open thereby configuring switched integrator 32 as an integrator, which may be used in a MASH configuration as will be more particularly described with reference to FIGURE 3.

Stages 12, 14, and 16 each includes a multi-bit quantizer, or sub-ADC, and a feedback DAC. The sub-ADC outputs a coarse digital signal for the corresponding stage, and the feedback DAC converts the coarse digital signal into a coarse analog signal. According to the illustrated embodiment, the sub-ADCs quantize the integrated signal to generate coarse digital signals for each stage. The coarse digital signals may then be used to generate a digital output 24 comprising the information embedded in input analog signal 22.

The feedback DAC of each of the stages 12, 14, and 16 also receive control signal *SDM* that reconfigures the feedback circuit. According to the illustrated embodiment, if control signal *SDM* is high, the feedback loop of the feedback DAC is actualized. If control signal *SDM* is low, the feedback loop of the feedback DAC is left open. At the feedback loop of the feedback DAC of first stage 12 and second stage 14, coarse analog signal 26 of the corresponding stage is summed with the integrated/sampled signal 28 of that stage to prepare the signal for feeding to the subsequent stage. At final stage 16, the feedback DAC may be omitted according to control signal *SDM*. For example, if control signal SDM is low, the feedback DAC may be omitted. If control

signal SDM is high, the feedback DAC operates to generate coarse analog signal 26 for summing with the amplified residual signal of the previous stage, in this case, middle stage 14.

Interstage gain block *G* is used to amplify and buffer a residual signal 30 for the next stage. According to the illustrated embodiment, residual signal 30 comprises the sum of coarse analog signal 26 and integrated/sampled signal 28. Interstage gain block *G* may amplify residual signal 30 according to a gain described by Equation (1):

$$G_{(n-1)n} \leq 2^{mn-1} \qquad (1)$$

where *n* represents the number of stages and *m* represents the number of bits generated per stage. Any other suitable gain may be applied to residual signal 30 without departing from the scope of the invention.

Digital logic 18 receives the coarse digital signals of stages 12, 14, and 16 to generate a digital output 24. According to the illustrated embodiment, digital logic may perform decimation, error correction, filtering, or any other suitable processing of a digital signal in order to generate a digital output. For example, in the embodiment where control signal *SDM* is low, digital logic 18 may perform digital error correction of the coarse digital signals to generate the digital output.

According to the illustrated embodiment, digital logic 18 generates the digital output in binary words *b<N-1,0>*, where *N* describes the total number of bits obtained as described by Equation (2):

$$N \approx \sum_{i=1}^{n} (mi-1) \qquad (2)$$

Depending on whether control signal *SDM* is high or low, the configuration of reconfigurable ADC 10 may toggle between a pipeline ADC or a MASH-like sigma-delta modulator. As will be described with reference to FIGURES 2 and 3, if control signal *SDM* is low, the configuration is that of a pipeline ADC, and if control signal SDM is high, the configuration is that of a MASH-like sigma-delta modulator. Accordingly, reconfigurable ADC 10 may operate at either a Nyquist frequency rate or an oversampling frequency rate depending on the configuration.

Modifications, additions, or omissions may be made to reconfigurable ADC 10 without departing from the scope of the invention. For example, additional middle stages 14 may be added to accommodate any suitable number of bits at digital output 24. As another example, reconfigurable ADC 10 may be expanded to include any suitable number of stages without departing from the scope of the invention. Additionally, functions may be performed using any suitable logic comprising software, hardware, other logic, or any suitable combination of the preceding. "Each" as used in this document refers to each member of a set or each member of a subset of a set.

A block diagram of one embodiment of a pipeline configuration that may be used with the reconfigurable analog-to-digital converter of FIGURE 1 is described with reference to FIGURE 2. A block diagram of one embodiment of a multi-stage noise shaping (MASH) ADC that may be

used with the reconfigurable analog-to-digital converter of FIGURE 1 is described with reference to FIGURE 3.

FIGURE 2 illustrates a block diagram of a pipeline ADC 40 that may result in response to a low control signal *SDM* received at the reconfigurable ADC 10 of FIGURE 1. According to one embodiment, pipeline ADC 40 comprises stages 12, 14, and 16 as described with reference to FIGURE 1. In the illustrated embodiment, middle stage 14 may include any number of sub-stages to accommodate any suitable number of bits at digital output 24 as was previously described. Pipeline ADC 40 may be used when the resolution required at a circuit may call for a moderate frequency rate, such as a Nyquist rate, and a high bandwidth.

In this embodiment, the integrator of first stage 12 is configured as a sample/hold circuit, while the integrators of subsequent stages 14 and 16 are configured as buffers. According to the illustrated embodiment, the buffers at the subsequent stages are gainless buffers.

At each stage, an analog input is either sampled and held or buffered and then transmitted to a sub-ADC module that converts the sampled/buffered signal into a coarse digital signal 42. According to one embodiment, a multi-bit ADC may be used to quantize the sampled/buffered signal and generate coarse digital signal 42. Any suitable technique for converting the sampled/buffered signal into coarse digital signal 42 may be used without departing from the scope of the invention. A DAC at each stage converts coarse digital signal 42 into coarse analog 44 signal that may be fed into a summing node. According to the illustrated embodiment, a DAC is not

used at final stage 16 according to control signal *SDM* as was described with reference to FIGURE 1.

At the end of each stage, a summing node Σ may generate a residual signal 46 by summing the sampled/buffered signal and coarse analog signal 44. Residual signal 46 may be described as the residual error of the stage, which may be amplified at the beginning of the subsequent stage to return the amplitude of the signal to a full-scale amplitude. As was described with reference to FIGURE 1, an internode gain block *G* at the beginning the stage amplifies the residual signal.

Digital error correction block 48 receives the course digital signal 42 from each stage to generate digital output 24. According to the illustrated embodiment, coarse digital signal 42 from stages 12, 14, and 16 are fed to digital error correction block 48 to perform error correction of the coarse digital signals 42 and generate digital output 24. Any suitable number of stages may be used to generate any suitable number of bits of coarse digital signal 42 without departing from the scope of the invention.

Modifications, additions, or omissions may be made to reconfigurable ADC 10 without departing from the scope of the invention. For example, although a four-stage reconfigurable ADC has been used to describe the configuration of pipeline ADC 40, additional stages may be added to middle stage 14 to accommodate any suitable number of bits at digital output 24. Additionally, functions may be performed using any suitable logic comprising software, hardware, other logic, or any suitable combination of the preceding.

FIGURE 3 illustrates a block diagram of a MASH-like sigma-delta modulator with interstage gain that may result in response to a high control signal *SDM* received at the reconfigurable ADC 10 of FIGURE 1. According to one embodiment, MASH-like sigma-delta modulator 50 comprises stages 12, 14, and 16 as described with reference to FIGURE 1. In the illustrated embodiment, middle stage 14 may include any number of sub-stages to accommodate a suitable number of bits at digital output 24 as was previously described. MASH-like sigma-delta modulator 50 may be used when the resolution required at a circuit may call for a high frequency rate, such as an oversampling rate, and a narrow bandwidth.

In this embodiment, each stage comprises a sigma-delta modulator such as a first order sigma-delta modulator. Higher order sigma-delta modulators may be used without departing from the scope of the invention. Additionally, at the beginning of each stage an interstage gain block *G* is included to amplify a residual analog signal 56 of the previous stage.

In operation, MASH-like sigma-delta modulator 50 receives input analog signal 22, and summation nodes Σ_1, integrators 32, and sub-stage ADCs (sub-ADCs) generate a coarse digital signal 52. According to one embodiment, coarse digital signal 52 may comprise a multi-bit digital signal. Coarse digital signal 52 may, however, comprise a one-bit digital signal. A feedback DAC circuit converts coarse digital signal 52 into a coarse analog signal 54. Summation node Σ_2 sums the coarse digital signal 52 and an integrated signal to generate residual analog signal 56 for the stage.

A decimation and low-pass filter block 58 receives the coarse digital signals 52 and converts them to a digital output 24. According to the illustrated embodiment, decimation and low-pass filter block 58 decimates and filters the coarse digital signals 52 to generate digital output 24 comprising the information embedded in analog input signal 22. Decimation and low-pass filter block 58 may perform other signal processing of coarse digital signals 52 suitable for generating digital output 24. For example, decimation and low-pass filter block 58 may also perform error correction.

Modifications, additions, or omissions may be made to reconfigurable ADC 10 without departing from the scope of the invention. For example, although a four-stage reconfigurable ADC has been used to describe the configuration of MASH-like sigma-delta modulator 50, an number of stages may be used at middle stage 14 to accommodate any suitable number of bits at digital output 24. Additionally, functions may be performed using any suitable logic comprising software, hardware, other logic, or any suitable combination of the preceding.

Certain embodiments of the invention may provide one or more technical advantages. A technical advantage of one embodiment may be the simplified hardware of a circuit that requires the use of various types of ADC resolution. Another technical advantage of one embodiment may be that by reconfiguring an ADC using a control signal, the reconfiguration may be more efficient.

Although an embodiment of the invention and its advantages are described in detail, a person skilled in the art could make various alterations, additions, and

omissions without departing from the spirit and scope of the present invention as defined by the appended claims.